CLAIMS

What is claimed is:

1. A monolithic structure, comprising:

a semiconductor substrate having a first surface;

one or more first lateral device having a first source terminal, a first drain terminal and a first gate terminal; said first source, drain and gate terminals terminating on said first surface;

one or more second lateral device having a second source terminal, a second drain terminal and a second gate terminal; said second source, drain and gate terminals terminating on said first surface; and;

said one or more first lateral device being combined with said one or more second lateral power transistor device on said substrate.

2. The monolithic structure of claim 1 further comprising at least one first electrically isolated lead comprising said first source terminal being connected to said second source terminal.

3. The monolithic structure of claim 2 further comprising at least one second and third electrically isolated leads comprising said first and second drain terminals; wherein said first and second drain terminals being electrically independent of each other.

4. The monolithic structure of claim 3 further comprising at least one third and fourth electrically isolated leads comprising said first and second gate terminals; wherein said first and second gate terminals being electrically independent of each other.

5. The monolithic structure of claim 3 wherein said first gate terminal being connected to said second drain terminal; said second gate terminal being connected to said first drain terminal.

6. The monolithic structure of claim 1 wherein each of said first and second lateral devices is a lateral power MOSFET.

7. A monolithic structure comprising at least two lateral power transistor devices combined on a semiconductor substrate, said structure comprising;

a semiconductor substrate having a first surface;

a first lateral power transistor device having a first source terminal, a first drain terminal and a first gate terminal; said first source, drain and gate terminals terminating on said first surface;

a second lateral power transistor device having a second source terminal, a second drain terminal and a second gate terminal; said second source, drain and gate terminals terminating on said first surface;

said first gate terminal being connected to said second drain terminal; said second gate terminal being connected to said first drain terminal; said first and second drain terminals being electrically independent of each other;

a first electrically isolated lead comprising said first source terminal being connected to said second source terminal;

a second electrically isolated lead comprising said first drain terminal; and

a third electrically isolated lead comprising said second drain terminal.

8. The monolithic structure of claim 7 wherein each of said first and second lateral power transistor devices is a lateral power MOSFET.

9. A monolithic structure comprising at least two lateral power transistor devices combined on a semiconductor substrate, said structure comprising;

a semiconductor substrate having a first surface;

a first lateral power transistor device having a first source terminal, a first drain terminal and a first gate terminal; said first source, drain and gate terminals terminating on said first surface;

a second lateral power transistor device having a second source terminal, a second drain terminal and a second gate terminal; said second source, drain and gate terminals terminating on said first surface;

said first and second drain terminal being electrically independent of each other;

a first electrically isolated lead comprising said first source terminal being connected to said second source terminal;

a second electrically isolated lead comprising said first drain terminal;

a third electrically isolated lead comprising said second drain terminal; and

a fourth electrically isolated lead comprising said first gate terminal being connected to said second gate terminal.

10. The monolithic structure of claim 9 wherein each of said first and second lateral power transistor devices is a lateral power MOSFET.

11. The monolithic structure of claim 9 wherein said second lateral power transistor is of substantially smaller size than said first lateral power transistor.

12. The monolithic structure of claim 9 wherein said first and second lateral power transistors each have substantially different threshold voltages; said difference in threshold voltages ranging from approximately 0.1V and greater.

13. A monolithic structure comprising at least two lateral power transistor devices combined on a semiconductor substrate, said structure comprising;

a semiconductor substrate having a first surface;

a first lateral power transistor device having a first source terminal, a first drain terminal and a first gate terminal; said first source, drain and gate terminals terminating on said first surface;

a second lateral power transistor device having a second source terminal, a second drain terminal and a second gate terminal; said second source, drain and gate terminals terminating on said first surface;

said first and second gate terminals being electrically independent of each other; and; said first and second drain terminal being electrically independent of each other;

a first electrically isolated lead comprising said first source terminal being connected to said second source terminal;

a second electrically isolated lead comprising said first drain terminal;

a third electrically isolated lead comprising said second drain terminal;

a fourth electrically isolated lead comprising said first gate terminal; and

a fifth electrically isolated lead comprising said second gate terminal.

14. The monolithic structure of claim 13 wherein each of said first and second lateral power transistor devices is a lateral power MOSFET.

15. The monolithic structure of claim 13 wherein said second lateral power transistor is of substantially smaller size than said first lateral power transistor.

16. The monolithic structure of claim 13 wherein said first and second lateral power transistors each have substantially different threshold voltages; said difference in threshold voltages ranging from approximately 0.1V and greater.